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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/739,758	12/20/2000	Takao Watanabe	HIT 2 482-06	7380

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EXAMINER	
HIRL, JOSEPH P	

ART UNIT	PAPER NUMBER
2121	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/739,758	WATANABE ET AL.	
	Examiner	Art Unit	
	Joseph P. Hirl	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to an AMENDMENT entered December 1, 2004 for the patent application 09/739,758 filed on December 20, 2000.

2. All prior office actions are fully incorporated into this Final Office Action by reference.

Status of Claims

3. Claim 25 and 29 are amended. Claims 25-37 are pending.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 29-37 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Substitute specification at page 13, lines 14-34 and page 14, lines 1-35 (substitute specification) describes Fig. 1 wherein:

a. The third bus does not write information from outside the semiconductor chip to the first memory array.

b. Only one section of memory identified as "A" is shown ... no first memory array, no second memory array.

c. In the interview of January 29, 2004, the Applicant specifically identified in the submitted agenda that the "first mode" corresponds to the memory mode. However, on page 14 at lines 5-9 (substitute specification), the first method (first mode?) is identified as one of calculating the neuron output values.

d. Although latch circuits can be flip-flops holding a line state, the text refers to such operation as writing in memory through the input/output circuit which does not require such latch circuits on page 14 at line 13 (substitute specification).

The result of the claim statements either teach a different concept, a counter concept or a concept that many not function given the disclosure of the specification.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

Claims 25-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Mashiko (U. S. Patent 4,988,891 referred to as **Mashiko**).

Claim 25

Mashiko anticipates a memory array having a plurality of word lines, a

plurality of bit lines, and a plurality of memory cells (**Mashiko**, col 1, lines 17-34; col 4, lines 17-24; col 3, lines 52-61); a processing circuit which carries out an operation using information stored in said memory array (**Mashiko**, col 2, lines 42-56); an input/output circuit (**Mashiko**, col 5, lines 27-59); wherein said semiconductor integrated circuit device has a first mode and a second mode (**Mashiko**, col 3, lines 51-61; col 5, lines 27-67; col 6, lines 1-2; Examiner's Note: the applicant does not specifically identify a first and second mode but applicant has an operation involving memory and an operation involving arithmetic (processing) and hence there can be two modes although the significance of one and two are in name only), wherein in said first mode read operation and write operation to said memory array are performed (**Mashiko**, col 6, lines 17-36), wherein the information stored in said memory array is read out to said input/output circuit in said read operation of said first mode and information outputted from said input/output circuit is written in said memory array in said write operation of the first mode (**Mashiko**, col 3, lines 37-51; col 6, lines 17-36), wherein in said second mode information stored in said memory array is read from said memory array to said processing circuit (**Mashiko**, Fig. 5) wherein said processing circuit has an arithmetic unit and a MOS transistor which has a source/drain path between said arithmetic unit and a power line and a gate inputted with a control signal (**Mashiko**, col 2, lines 64-67; col 3, lines 1-6; col 15, lines 42-43), and wherein during said first mode said MOS transistor is in an OFF state (**Mashiko**, Fig. 17; EN: the signals at 340 are either off or on).

Claim 26

Mashiko anticipates input/output circuit is for inputting and outputting data from and to outside of said semiconductor chip (**Mashiko**, col 2, lines 37-67; col 3, lines 1-6), and wherein a signal from outside said semiconductor integrated circuit controls whether said semiconductor circuit is in the first mode or second mode (**Mashiko**, col 2, lines 42-56; EN: the control signal is in the form of the presence of data at the input which will cause the semiconductor to execute the first and second modes).

Claim 27

Mashiko anticipates a plurality of memory arrays, wherein each of the plurality of memory cells includes a MOS transistor and a capacitor, and wherein said processing circuit is formed by MOS transistors (**Mashiko**, col 15, lines 53-67; EN: Fig. 1 is a representation of a neuron. Fig. 4 is a schematic of a neural network. Col 4, lines 17-24 identify the transition from the neuron to the neural network. Neural networks have memory that resides in the network...weights and interconnectivity. The circuit implementation of Fig. 4 uses electronic solid state components to achieve the VLSI configuration of column 2, lines 37-41. **Mashiko** implements his invention using Metal Oxide Semiconductors (MOS) and other generic electronic components such as capacitors such as those components identified in col 15, lines 42-52), wherein one of said plurality of memory arrays is selected in said first mode (**Mashiko**, Fig.5), and wherein said arithmetic unit is placed between two of said plurality of said memory arrays and receives outputs from said two of said plurality of memory arrays (**Mashiko**, Fig.5; EN: the circuit associated with the Random Access Memory is equivalent to an

arithmetic unit since depending on the signal input, the circuit proportionally adjusts values of voltage and current.).

Claim 28

Mashiko anticipates each of the plurality of memory cells includes a MOS transistor and a capacitor, and said processing circuit is formed by MOS transistors, and wherein said semiconductor integrated circuit device is formed on a semiconductor chip (**Mashiko**, col 15, lines 53-67; EN: Fig. 1 is a representation of a neuron. Fig. 4 is a schematic of a neural network. Column 4, lines 17-24 identify the transition from the neuron to the neural network. Neural networks have memory that resides in the network...weights and interconnectivity. The circuit implementation of figure 4 uses electronic solid state components to achieve the VLSI configuration of column 2, lines 37-41. Mashiko implements his invention using Metal Oxide Semiconductors (MOS) and other generic electronic components such as capacitors and those components identified in column 15, lines 42-52; to one of ordinary skill in the art, a semiconductor integrated circuit is formed on a semiconductor chip; **Mashiko**, col 3 lines 4-5).

Claim 29

Mashiko anticipates a first memory array including a plurality of DRAM memory cells (**Mashiko**, col 3, lines 52-61; EN: DRAM is dynamic RAM which is random access memory); a logic circuit coupled to said first memory array (**Mashiko**, col 2, lines 42-56; EN: row decoders, bit decoders, registers have logic circuits of a plurality degree implemented with generic MOS transistors); an input/output circuit including latch

circuits (**Mashiko**, col 5, lines 27-67; col 2, lines 64-68); a first bus coupled between said first memory array and said logic circuit (**Mashiko**, col 2, lines 37-56; col 3, lines 7-22; Figs. 3, 4, 5; EN: memory array is register; input lines represent a bus); a second bus coupled between said logic circuit and said input/output circuit (**Mashiko**, col 2, lines 37-56; col 3, lines 7-22; Figs. 3, 4, 5; EN: memory array is a register; output lines represent a bus); and a third bus coupled between said first memory array and said input/output circuit (**Mashiko**, col 2, lines 37-56; col 3, lines 7-22; Figs. 3, 4, 5; EN: memory array is a register; input/output circuit is a register; programmed lines from exterior to set the resistive coupling represent a bus); wherein said semiconductor integrated device has a first mode and a second mode (**Mashiko**, col 3, lines 51-61; col 5, lines 27-67; col 6, lines 1-2; Examiner's Note: the applicant does not specifically identify a first and second mode but applicant has an operation involving memory and an operation involving arithmetic (processing) and hence there can be two modes although the priority significance of one and two is in name only as described by the applicant), wherein in said first mode, by using said third bus, information from outside said semiconductor chip is written to said first memory array or information stored in said first memory array is read out of said semiconductor chip from said first memory array (**Mashiko**, col 2, lines 37-56; col 3, lines 7-22; Figs. 3, 4, 5; EN: memory array is a register; input/output circuit is a register; programmed lines from exterior to set the resistive coupling will be read to the respective resistive coupling); wherein in said second mode, by using said first bus, information is read from said first memory array to said logic circuit, by using said second bus, said logic circuit outputs results of said

operation to said latch circuit, and by using said third bus, data in accordance with said results is written to said first memory array (**Mashiko**, col 2, lines 37-56; col 3, lines 7-22; Figs. 3, 4, 5; EN: programmed information re third bus will influence the output data that is written to the register ... input/output)

Claim 30

Mashiko anticipates a second memory array including a plurality of DRAM memory cells coupled to said logic circuit and said input/output circuit , wherein said logic circuit is placed between said first memory array and said second memory array and receives outputs said first memory array and said second memory array (**Mashiko**, col 2, lines 37-67; col 3, lines 52-61; EN: specification at Fig. 1 does not have a second memory array).

Claim 31

Mashiko anticipates a converting circuit which converts said results to said data so that a number of bits used for said data is equal to a number of bits used for information read out to said logic circuit, wherein each of the plurality of DRAM memory cells includes a MOS transistor and a capacitor (**Mashiko**, col 2, lines 37-67; col 3, lines 52-61; Figs. 6- EN: see comments of claim 28; the converting circuit as claimed is a non event; specifically if the case is represented by a binary design and there are N bits on the input and N bits on the output, to one of ordinary skill in the art, there has been no conversion...each input bit equals each output bit).

Claims 32

Mashiko anticipates each of the plurality of DRAM memory cells includes a MOS transistor and a capacitor (**Mashiko**, col 2, lines 37-67; col 3, lines 52-61; Figs. 5-8; EN: above comments apply).

Claim 33

Mashiko anticipates mode changing between said first mode and said second mode is performed in accordance with a signal from outside of said semiconductor chip (**Mashiko**, col 2, lines 37-67; col 3, lines 52-61; EN: typically, as information is received from an outside source, it is stored in memory and then processed as necessary following the appearance of the outside information).

Claim 34

Mashiko anticipates said logic circuit includes an arithmetic unit and a MOS transistor which has a source/drain path between said arithmetic unit and a power line (**Mashiko**, Fig. 17), and wherein during said first mode said MOS transistor is in off condition (**Mashiko**, Fig. 17; EN: the modes as such are not defined in the specification and therefore the claim is being interpreted as indicating that at sometime, under some condition, the transistor is off which, from the figure, such is the case).

Claim 35

Mashiko anticipates a comparing circuit comparing said results with an expected value (**Mashiko**, col 6, lines 1-2).

Claim 36

Mashiko anticipates a register coupled between said first memory array and said logic circuit (**Mashiko**, Fig. 8A), wherein in said second mode read operation and write operation against first memory array is performed concurrently (**Mashiko**, Fig. 8A; EN: to one of ordinary skill in the art, parallel processing against a register (memory array) will always be done in a concurrent manner).

Claim 37

Mashiko anticipates first memory array and second memory array each includes sense amplifiers and a precharged circuit (**Mashiko**, col 3, lines 28-51; EN: sets of RAM 1 constitutes first memory array; sets of Ram 2 constitutes RAM 2; all amplifiers sense their input; all circuits are precharged upon initialization to initial conditions).

Response to Arguments

6. Applicant's arguments filed on December 1, 2004 related to Claims 25-37 have been fully considered but are not persuasive.

In reference to Applicant's argument:

35 U.S.C. §112

The Examiner's rejection of claims 29-37 under this section for failing to comply with the enablement requirement is apparently based upon the Examiner's attempt to read these claims only on Fig. 1 and its corresponding description-in the specification. However, the subject matter of claims 29-37 mainly finds support in Figs. 11-14 and their corresponding description. Applicants wish to direct to Examiner's attention to the discussion of the personal interview that was contained in a response filed January 30, 2004, in which Figs. 11, 13 (a) and 13 (b) are cited for support of the first mode and the second mode that are being claimed. As such, Applicants once again request that the Examiner focus on these figures to assist in understanding the claim language.

Examiner's response:

In the substitute specification @ pages 13, line 14:

Fig. 1 shows one embodiment in the case where the data processing system according to the present invention is integrated over a semiconductor chip.

The text then goes on to further discuss the operations of the related semiconductor chip over the next several pages without ever making any reference to Figs. 11, 13(a) or 13(b). Further, the applicant is reminded that personal interview material is not specification material and can be considered new matter. The disclosure under examination consists of: specification, drawings and claims.

In reference to Applicant's argument:

Applicants respond to each of the Examiner's points as follows. With respect to item 5(a) of the Office Action, Applicants respond that the third bus corresponds to OA and IA as shown in Fig. 11. OA is a read line and IA is a write line (see page 39, lines 26-30 and page 41, lines 13-15). Therefore, it is submitted that the specification more than adequately describes that information from outside the semiconductor chip is written to a first memory array A via a third bus. With respect to item 5(b) the first memory array and the second memory array correspond to arrays A and B shown in Fig. 11. With respect to item 5(c) the first mode corresponds to the memory mode in Fig. 12. Finally, with respect to item 5(d) the latch circuit corresponds to LAT in Fig. 14(c). In conclusion, if the claims are properly read in light of the specification, particularly the portions mentioned above, there should be no question as to whether the enablement requirement is satisfied.

Examiner's response:

Applicant has not addressed the examiner's comments of the Office Action dated July 1, 2004 related to substitute specification pages 13 and 14 to which the concerns of 5a. to 5d. were written. While the applicant's reference to specification, lines 26-30 does reference read line OA, there is no reference to IA on page 39 or 41 of the substitute specification. Further, the cited references do not relate to Fig. 11. Concerning 5b., Fig. 1 identifies only memory A. Applicant has not identifies any text

that identifies the related sections of Fig. 11 that directly relate to a first memory array and a second memory array. Page 29, lines 24-30 does address array A and array B but there is no identification of first memory array and a second memory array. Concerning 5c., there is no notation in Fig. 12 to indicate that the memory mode is the first mode. Concerning 5d., while Fig. 14(c). has a latch circuit , it is not clear why the first embodiment elects to function without such circuitry. Isn't simplicity better than complexity? Latching is not the "best " implementation? The claims and the specification appear to be at odds raising the question of enablement. If the claims followed a "means for" related to the specification, the concept would be enabled.

In reference to Applicant's argument:

35 U.S.C. §102

Independent claim 25 is directed to a semiconductor integrated circuit device in which, in a first mode, a read operation and a write operation to the memory array are performed. Furthermore, the information stored in the memory array is read out to an input/output circuit in the read operation of the first mode and information outputted from the input/output circuit is written to the memory array in the write operation of the first mode.

The Examiner asserts that Mashiko discloses this feature of the claimed invention at column 3, lines 37-51 and column 6, lines 17-36. However, this portion of Mashiko merely discloses that random access memory cells 150 and 151 can be programmed from the exterior, but does riot mention anything about reading out from RAM 150 and 151.

Examiner's response:

From Mashiko @ c3, l 37-51: "The on/Off state of the switching element S3 is set by information stored in the random access memory cell 151. " To execute such an operation, RAM 151 has to be read.

In reference to Applicant's argument:

Independent claim 25 also recites that a MOS transistor of a processing circuit which has a source/drain path between the arithmetic unit and a power line and a gate inputted with a control signal is in an OFF state during the first mode. The Examiner attempt to rely upon Fig. 7.7 of Mashiko to disclose this feature is incorrect. Fig. 17 of Mashiko merely shows a driving circuit for a liquid crystal shutter array (see column 15, lines 42-53). Item 310 in Fig. 17 is a TN type liquid crystal cell and is not a processing circuit as recited in the pending claims (see column 15, lines 42-52).

Examiner's response:

Related to Fig. 17, Mashiko @ c 15, l 41-52 cites the circuitry to include MOS transistor 330. The MOS transistor is connected via the source/drain to a power line and an arithmetic unit being the program data and the signal electrode driving circuit, which does arithmetic operations. Since without power would be its first mode, the gate signal would be in an off state. Office Action of July 1, 2004 applies.

In reference to Applicant's argument:

It is also submitted that independent claim 29 patentably defines the present invention over Mashiko. The Examiner states that the plurality of DRAM memory cells in claim 29 correspond to the RAM in Fig. 5 of Mashiko and that a third bus corresponds to programmed lines from the exterior. The Examiner further states that "programmed information re third bus will influence the output data that is written to the register . . . input/output". However, Mashiko discloses that the input/output data register is coupled to input lines and output lines, but does not disclose that programmed lines for the RAM are coupled to the input/output data register. Furthermore, the input lines and the out put lines are not coupled to the RAM.

Examiner's response:

The requirements stated by the applicant are not part of the claim 29 limitations.

In reference to Applicant's argument:

Therefore, Mashiko merely suggests in column 3, lines 52-58 how to select the RAM, but does not mention which lines are used to transfer programmed information to the RAM. Possibly, the programmed information is transferred to the RAM of Mashiko via the bit lines in Fig. 5. Therefore, the programmed information is likely transferred from the bit decoder to the RAM, and not from the input/output data register to the RAM. Therefore, the programmed information for the RAM will not influence the output data that is written to the register.

Examiner's response:

Again, the requirements stated by the applicant are not part of the claim 29 limitations. Applicant is reminded that it is the claims and only the claims that define the metes and bounds of the invention.

In reference to Applicant's argument:

The input lines and output lines correspond to lines A and B shown in Fig. 4 (see column 3, lines 7-8). In addition, the input lines Al to A4 are respectively provided with amplifiers C1 to C4 which amplify the data on the corresponding input lines and transmit the same on to the corresponding output lines (see column 3, lines 24-27). Therefore, the input lines and the output lines are not coupled to the RAM. Instead, the RAM is merely coupled to word lines WL1, WL2 and BL.

Examiner's response:

The issue is: "What does the applicant's claims cite as limitations?" The above discussion by the applicant is not to be found in the related claims. The applicant is further reminded that: "Limitations appearing in the specification but not recited in the claim are not read into the claim."

Examination Considerations

7. The claims and only the claims form the metes and bounds of the invention. "Office personnel are to give the claims their broadest reasonable interpretation in light of the supporting disclosure. *In re Morris,* 127 F.3d 1048, 1054-55, 44USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. *In re Prater*, 415 F.2d, 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969)" (MPEP p 2100-8, c 2, l 45-48; p 2100-9, c 1, l 1-4). The Examiner has full latitude to interpret each claim in the broadest reasonable sense.

Examiner will reference prior art using terminology familiar to one of ordinary skill in the art. Such an approach is broad in concept and can be either explicit or implicit in meaning.

8. Examiner's Notes are provided to assist the applicant to better understand the nature of the prior art, application of such prior art and, as appropriate, to further indicate other prior art that maybe applied in other office actions. Such comments are entirely consistent with the intent and spirit of compact prosecution. However, and unless otherwise stated, the Examiner's Notes are not prior art but a link to prior art that one of ordinary skill in the art would find inherently appropriate.

9. Examiner's Opinion: Paras 7. and 8. apply. The Examiner has full latitude to interpret each claim in the broadest reasonable sense.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Claims 25-37 are rejected.

Correspondence Information

12. Any inquiry concerning this information or related to the subject disclosure should be directed to the Examiner, Joseph P. Hirl, whose telephone number is (571) 272-3685. The Examiner can be reached on Monday – Thursday from 6:00 a.m. to 4:30 p.m.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Anthony Knight can be reached at (571) 272-3687. Any response to this office action should be mailed to:

Commissioner of Patents and Trademarks,

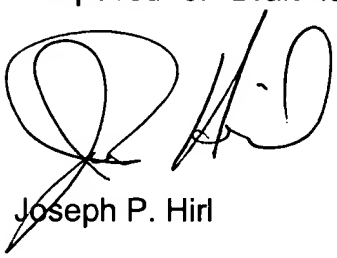
Washington, D. C. 20231;

or faxed to:

(703) 872-9306 (for formal communications intended for entry);

or faxed to:

(571) 273-3685 (for informal or draft communications with notation of "Proposed" or "Draft" for the desk of the Examiner).



Joseph P. Hirl

February 8, 2005